CUSTOMER NO.
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CLAIM LISTING

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claim 1, and add new claims 21-23 such that pending claims 1-23 read as follows:

1. (Currently Amended) A buffer comprising:

a capacitor having a first terminal for receiving an input signal, and a second terminal;

a first transistor comprising a low-voltage transistor having a first current electrode coupled to a first power supply voltage terminal for receiving a first power supply voltage, a control electrode coupled to said second terminal of said capacitor, and a second current electrode for providing an output signal of the buffer;

a second transistor comprising a low-voltage transistor having a first current electrode coupled to said second current electrode of said first transistor, a control electrode coupled to said second terminal of said capacitor, and a second current electrode coupled to a second power supply voltage terminal for receiving a second power supply voltage;

wherein said input signal has a peak-to-peak voltage swing equal to a first voltage;

wherein a voltage difference between said first power supply voltage and said second power supply voltage is equal to a second voltage that is lower than said first voltage; and

wherein a capacitance of said capacitor is chosen such that a peak-to-peak voltage swing at said control electrodes of said first and second transistors is less than or equal to said second voltage.

2. (Original) The buffer of claim 1, further comprising:

a resistor having a first terminal coupled to said second terminal of said capacitor, and a second terminal coupled to said second current electrode of said first transistor.

3. (Original) The buffer of claim 1, wherein said first and second transistors comprise metal oxide semiconductor (MOS) field effect transistors.

4. (Original) The buffer of claim 3, wherein said first transistor comprises a P-channel MOS field effect transistor and said second transistor comprises an N-channel MOS field effect transistor.

5. (Original) The buffer of claim 1, wherein said first and second transistors are characterized as having an oxide stress voltage less than said first voltage.

6. (Original) The buffer of claim 5, wherein said first and second transistors are characterized as having a gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process.

7. (Original) The buffer of claim 7, wherein said first voltage is about 3.5 volts, and said second voltage is about 1.2 volts.

8. (Original) A circuit comprising:

a signal source having an output terminal for providing a time-varying signal having a peak-to-peak signal swing equal to a first voltage; and

a buffer coupled to first and second power supply voltage terminals for respectively receiving first and second power supply voltages thereon, and having an input terminal coupled to said output terminal of said signal source, and an output terminal;

a difference between said first and second power supply voltages being equal to a second voltage that is less than said first voltage;

wherein said buffer comprises:

a capacitor having a first terminal coupled to said output terminal of said signal source, and a second terminal;

a first transistor having a first current electrode coupled to said first power supply voltage terminal, a control electrode coupled to said second terminal of said capacitor, and a second current electrode for providing an output signal of said buffer;

a second transistor having a first current electrode coupled to said second current electrode of said first transistor, a control electrode coupled to said second terminal of said capacitor, and a second current electrode coupled to said second power supply voltage terminal;

wherein a capacitance of said capacitor is chosen such that a peak-to-peak voltage swing at said control electrodes of said first and second transistors is less than or equal to said second voltage.

9. (Original) The circuit of claim 8, further comprising:

an interconnect line having a first end coupled to said output terminal of said buffer, and a second end; and

a load coupled to said second end of said interconnect line.

10. (Currently Amended) The circuit of claim 9, wherein said load comprises:

a capacitor having a first terminal coupled to said second end of said interconnect line, and a second terminal coupled to said ~~said~~ second power supply voltage terminal.

11. (Original) The circuit of claim 8, wherein said buffer further comprises:

a resistor having a first terminal coupled to said second terminal of said capacitor, and a second terminal coupled to said second current electrode of said first transistor.

12. (Original) The circuit of claim 8, wherein said first and second transistors comprise metal oxide semiconductor (MOS) field effect transistors.

13. (Original) The circuit of claim 12, wherein said first transistor comprises a P-channel MOS field effect transistor and said second transistor comprises an N-channel MOS field effect transistor.

14. (Original) The circuit of claim 11, wherein said first and second transistors are characterized as having an oxide stress voltage less than said first voltage.

15. (Original) The circuit of claim 14, wherein said first and second transistors are characterized as having a gate oxide thickness that is substantially a minimum thickness of an associated manufacturing process.

16. (Original) The circuit of claim 8, wherein said first voltage is about 3.5 volts, and said second voltage is about 1.2 volts.

17. (Original) A method of buffering an input signal having a peak-to-peak voltage equal to a first voltage comprising the steps of:

capacitively dividing the first voltage using a capacitive divider formed by a capacitor having a first terminal for receiving the input signal and a second terminal in series with a parasitic capacitance formed by control electrodes of first and second transistors to provide a second signal at said second terminal of said capacitor having a peak-to-peak voltage equal to a second voltage;

buffering said second signal using a buffer including said first and second transistors driven by a power supply voltage that is less than said first voltage and greater than or equal to said second voltage.

18. (Original) The method of claim 17, wherein said step of buffering comprises the step of:

buffering said second signal using said buffer in which said first transistor has a first current electrode coupled to said power supply voltage, a control electrode coupled to said second terminal of said capacitor, and a second current electrode coupled to a first current electrode of said second transistor which also has a control electrode coupled to said second terminal of said capacitor, and a second current electrode coupled to a second power supply voltage terminal.

19. (Original) The method of claim 17, further comprising the step of:

using an output of said buffer to drive a load coupled to said buffer through an interconnect line.

20. (Original) The method of claim 17, further comprising the step of:

biasing an input terminal of said buffer using a resistor coupled between an output terminal and said input terminal of said buffer.

21. (New) The buffer of claim 1, wherein the capacitance of the capacitor is greater than a combined parasitic capacitance of the first transistor and the second transistor.

22. (New) The circuit of claim 8, wherein the capacitance of the capacitor is greater than a combined parasitic capacitance of the first transistor and the second transistor.

23. (New) The circuit of claim 17, wherein the capacitor comprises a capacitance that is greater than the parasitic capacitance.